FPGA Configuration (1C)

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FPGA Configuration

The contents of this document is from the following documents

http://www-mtl.mit.edu/Courses/6.111/labkit/configuration.shtml
http://www.xilinx.com/itp/xilinx10/isehelp/ise_c_configuration_overview.htm
http://www.univ-st-etienne.fr/salware/Bibliography_Salware/FPGA%20Bistream%20Security/Article/Note2008.pdf
http://homepages.cae.wisc.edu/~ece554/new_website/ToolDoc/Xilinx_Fndtn_4.2i_docs/docs/pac/pac.pdf

FPGA Configuration

iMPACT
JTAG

TDI -> Compact Flash Controller -- FPGA -- PROM -> TDO

a. configure devices using Boundary-Scan (JTAG)
b. Prepare a PROM file
c. Prepare a SystemACE File
d. Prepare a Boundary-Scan File
e. Configure devices

Configuration Overview
After generating a programming file using the Generate Programming File process, you can configure your device, create PROM or System ACE files, or create SVF, XSVF, or STAPL files.

FPGA Configuration

PROM Files
Xilinx FPGAs are SRAM-based and must be programmed every time power is cycled. The most common method of programming Xilinx FPGAs is by using Xilinx PROMs connected to a chain of FPGAs. You must program these PROMs using PROM files created from the bitstreams of each FPGA in the configuration chain.
PROM files include information on the FPGA chain length and contain bitstreams that are reformatted for use with PROM programmers. Several PROM file formats are available: MCS, EXO, TEK, HEX, UFP, BIN, and ISC. iMPACT can directly program Xilinx PROM devices using MCS, EXO, and ISC file formats.

System ACE Files
Xilinx System Advanced Configuration Environment (ACE) files are used with the System ACE™ device family, which features greater capacity and flexibility than Xilinx PROMs. The System ACE CompactFlash (CF) solution allows you to program an FPGA target chain or chains. This configuration solution is a chipset, which comprises an ACE controller device and a CompactFlash storage device.

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Boundary Scan or JTAG Files
Boundary scan files, also known as JTAG files, are script files that describe a sequence of boundary scan commands and data. To create these script files, iMPACT records the sequence of boundary scan actions in iMPACT and writes these sequences to the script file. Following are the different file formats and their uses:

SVF and STAPL files

You can use serial vector format (SVF) files and STAPL files with automated test equipment (ATE) to test boards and to program Xilinx® devices before sending the boards to your customers.

XSVF files

You can use the Xilinx serial vector format (XSVF) file for embedded systems in which the FPGA is configured by an on-board microprocessor.

FPGA Configuration

The Configure Target Device process uses the output from the Generate Programming File process, a BIT, JEDEC or ISC file, to configure your target device.
The target device can be:

An FPGA -For FPGAs, the BIT and ISC files contain all of the configuration information from the NCD file, which defines the internal logic and interconnections of the device, plus device-specific information from other files associated with the target device. The binary data in the BIT or ISC file is downloaded to the FPGA memory cells.

References

[1] http://www-mtl.mit.edu/Courses/6.111/labkit/configuration.shtml
[2] http://www.xilinx.com/itp/xilinx10/isehelp/ise_c_configuration_overview.htm
[3] http://www.univ-st-etienne.fr/salware/Bibliography_Salware/FPGA%20Bistream%20Security/Article/Note2008.pdf
[4] http://homepages.cae.wisc.edu/~ece554/new_website/ToolDoc/Xilinx_Fndtn_4.2i_docs/docs/pac/pac.pdf